CTLDM8120-M621H

SURFACE MOUNT TLM™
P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET

Top View

Bottom View

TLM621H CASE

Central™
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM8120-M621H is a very low profile (0.4mm) P-Channel enhancement-mode MOSFET in a small, thermally efficient, 1.5mm x 2mm TLM™ package.

MARKING CODE: CNF

FEATURES:

- Device is ***Halogen Free*** by design
- Low $r_{DS(on)}$ (0.24Ω MAX. @ V_{GS}=1.8V)
- High Current (I_D=0.95A)
- Logic Level Compatible
- Small, 1.5 x 2.0 x 0.4mm Ultra Low Height Profile **TLM™**

APPLICATIONS:

- Load / Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

MAXIMUM RATINGS: (T_A=25°C)

	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	8	V
Continuous Drain Current (Steady State)	I_D	860	mA
Continuous Drain Current (t ≤ 5s)	I_D	950	mA
Continuous Source Current (Body Diode)	I_S	360	mA
Maximum Pulsed Drain Current (tp=10μs)	I_{DM}	4	A
Maximum Pulsed Source Current (tp=10μs)	I_{SM}	4	A
Power Dissipation (Note 1)	P_D	1.6	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	75	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}	V_{GS}=8.0V, V_{DS}=0V		1.0	50	nA
I_{GSSR}	V_{GS}=8.0V, V_{DS}=0V		1.0	50	nA
I_{DSS}	V_{DS}=20V, V_{GS}=0V		5.0	500	nA
BV_{DSS}	V_{GS}=0V, I_D=250μA	20	24		V

Notes: (1) Mounted on a 4-layer JEDEC test board with one thermal vias connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

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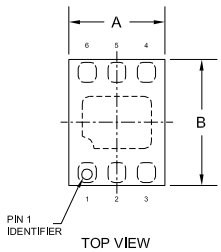
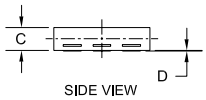
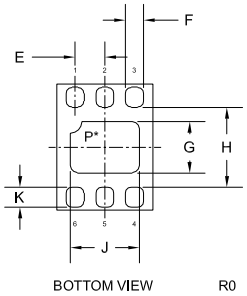
ELECTRICAL CHARACTERISTICS - Continued (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	0.45	0.76	1.0	V
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=0.95A		85	150	mΩ
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=0.77A		85	142	mΩ
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=0.67A		130	200	mΩ
$r_{DS(ON)}$	V_{GS}=1.8V, I_D=0.2A		190	240	mΩ
Y_{fs}	V_{DS} =10V, I_D=810mA	2.0			S
C_{rss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz		80		pF
C_{iss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz		200		pF
C_{oss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz		60		pF
t_{on}	V_{DD}=10V, V_{GS}=4.5V, I_D=950mA,		20		ns
t_{off}	R_G=6Ω		25		ns
V_{SD}	V_{GS}=0V, I_S=360mA			0.9	V

TLM621H CASE - MECHANICAL OUTLINE





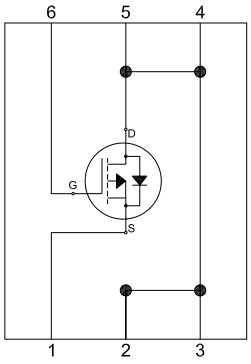


* Exposed pad P Internally connected to pins 3 and 4

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

TLM621H (REV:R0)

PIN CONFIGURATION
TOP VIEW



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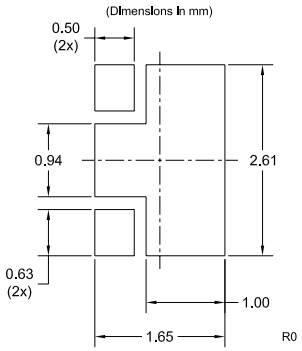
Optional Mounting Pad



For standard mounting refer to TLM621H Package Details

LEAD CODE:
1) SOURCE
2) DRAIN
3) DRAIN
4) DRAIN
5) DRAIN
6) GATE

R0 (22-May 2007)